

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 *     Zvector E7 instruction tests for VRR-c encoded:
				5 *
				6 *     E775 VSLB    - Vector Shift Left By Byte
				7 *     E77D VSRLB   - Vector Shift Right Logical By Byte
				8 *     E77F VSRAB   - Vector Shift Right Arithmetic By Byte
				9 *
				10 *           James Wekel March 2025
				11 *****
				13 *****
				14 *
				15 *           basic instruction tests
				16 *
				17 *****
				18 *     This program tests proper functioning of the z/arch E7 VRR-c vector
				19 *     Shift by Byte (left, right logical, right arithmetic) instructions.
				20 *
				21 *     Exceptions are not tested.
				22 *
				23 *     PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				24 *     obvious coding errors. None of the tests are thorough. They are
				25 *     NOT designed to test all aspects of any of the instructions.
				26 *
				27 *****
				28 *
				29 *     *Testcase zvector-e7-15-ShiftByByte
				30 *     *
				31 *     *     Zvector E7 instruction tests for VRR-c encoded:
				32 *     *
				33 *     *     E775 VSLB    - Vector Shift Left By Byte
				34 *     *     E77D VSRLB   - Vector Shift Right Logical By Byte
				35 *     *     E77F VSRAB   - Vector Shift Right Arithmetic By Byte
				36 *     *
				37 *     *     # -----
				38 *     *     #     This tests only the basic function of the instructions.
				39 *     *     #     Exceptions are NOT tested.
				40 *     *     # -----
				41 *     *
				42 *     main size        2
				43 *     numcpu           1
				44 *     sysclear
				45 *     archlvl         z/Arch
				46 *     *
				47 *     loadcore        "\$(testpath)/zvector-e7-15-ShiftByByte.core" 0x0
				48 *     *
				49 *     diag8cmd        enable     # (needed for messages to Hercules console)
				50 *     runtest          5
				51 *     diag8cmd        disable    # (reset back to default)
				52 *     *
				53 *     *Done
				54 *     *
				55 *****

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				57 *****
				58 * FCHECK Macro - Is a Facility Bit set?
				59 *
				60 * If the facility bit is NOT set, an message is issued and
				61 * the test is skipped.
				62 *
				63 * Fcheck uses R0, R1 and R2
				64 *
				65 * eg. FCHECK 134, 'vector-packed-decimal'
				66 *****
				67 MACRO
				68 FCHECK &BITNO, &NOTSETMSG
				69 . * &BITNO : facility bit number to check
				70 . * &NOTSETMSG : 'facility name'
				71 LCLA &FBBYTE Facility bit in Byte
				72 LCLA &FBBIT Facility bit within Byte
				73
				74 LCLA &L(8)
				75 &L(1) SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
				76
				77 &FBBYTE SETA &BITNO/8
				78 &FBBIT SETA &L((&BITNO-(&FBBYTE*8))+1)
				79 . * MNOTE 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
				80
				81 B X&SYSNDX
				82 * Fcheck data area
				83 * skip messgae
				84 SKT&SYSNDX DC C' Skipping tests: '
				85 DC C&NOTSETMSG
				86 DC C' (bit &BITNO) is not installed.'
				87 SKL&SYSNDX EQU *-SKT&SYSNDX
				88 * facility bits
				89 DS FD gap
				90 FB&SYSNDX DS 4FD
				91 DS FD gap
				92 *
				93 X&SYSNDX EQU *
				94 LA R0, ((X&SYSNDX- FB&SYSNDX)/8)-1
				95 STFLE FB&SYSNDX get facility bits
				96
				97 XGR R0, R0
				98 IC R0, FB&SYSNDX+&FBBYTE get fbit byte
				99 N R0, =F' &FBBIT' is bit set?
				100 BNZ XC&SYSNDX
				101 *
				102 * facility bit not set, issue message and exit
				103 *
				104 LA R0, SKL&SYSNDX message length
				105 LA R1, SKT&SYSNDX message address
				106 BAL R2, MSG
				107
				108 B EOJ
				109 XC&SYSNDX EQU *
				110 MEND

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				112	*****		
				113	* Low core PSWs		
				114	*****		
00000000		00000000	000019E3	115	ZVE7TST START 0		
		00000000		116	USING ZVE7TST, R0	Low core addressability	
		00000140	00000000	117			
				118	SVOLDPSW EQU ZVE7TST+X' 140'	z/Arch Supervisor call old PSW	
00000000		00000000	000001A0	120	ORG ZVE7TST+X' 1A0'	z/Architecture RESTART PSW	
000001A0	00000001 80000000			121	DC X' 0000000180000000'		
000001A8	00000000 00000200			122	DC AD(BEGIN)		
000001B0		000001B0	000001D0	124	ORG ZVE7TST+X' 1D0'	z/Architecture PROGRAM CHECK PSW	
000001D0	00020001 80000000			125	DC X' 0002000180000000'		
000001D8	00000000 0000DEAD			126	DC AD(X' DEAD')		
000001E0		000001E0	00000200	128	ORG ZVE7TST+X' 200'	Start of actual test program..	
				130	*****		
				131	* The actual "ZVE7TST" program itself...		
				132	*****		
				133	* Architecture Mode: z/Arch		
				134	* Register Usage:		
				135	* R0 (work)		
				136	* R1-4 (work)		
				137	* R5 Testing control table - current test base		
				138	* R6- R7 (work)		
				139	* R8 First base register		
				140	* R9 Second base register		
				141	* R10 Third base register		
				142	* R11 E7TEST call return		
				143	* R12 E7TESTS register		
				144	* R13 (work)		
				145	* R14 Subroutine call		
				146	* R15 Secondary Subroutine call or work		
				147	* *****		
				148	*****		
00000200		00000200		152	USING BEGIN, R8	FIRST Base Register	
00000200		00001200		153	USING BEGIN+4096, R9	SECOND Base Register	
00000200		00002200		154	USING BEGIN+8192, R10	THIRD Base Register	
00000200	0580			156	BEGIN BALR R8, 0	Inititalize FIRST base register	
00000202	0680			157	BCTR R8, 0	Inititalize FIRST base register	
00000204	0680			158	BCTR R8, 0	Inititalize FIRST base register	
00000206	4190 8800		00000800	160	LA R9, 2048(, R8)	Inititalize SECOND base register	
0000020A	4190 9800		00000800	161	LA R9, 2048(, R9)	Inititalize SECOND base register	
				162			



[illegible]

[illegible]









LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				329 *****
				330 *            Normal completion or Abnormal termination PSWs
				331 *****
00000448	00020001 80000000			333 E0JPSW    DC        0D' 0' , X' 0002000180000000' , AD(0)
00000458	B2B2 8248		00000448	335 E0J            LPSWE E0JPSW                    Normal completion
00000460	00020001 80000000			337 FAILPSW    DC        0D' 0' , X' 0002000180000000' , AD(X' BAD' )
00000470	B2B2 8260		00000460	339 FAILTEST    LPSWE FAILPSW                    Abnormal termination
				341 *****
				342 *            Working Storage
				343 *****
00000474	00000000			345 CTLR0        DS        F                    CRO
00000478	00000000			346                DS        F
0000047C				348                LTORG ,                    Literals pool
0000047C	00000040			349                        =F' 64'
00000480	00001998			350                        =A(E7TESTS)
00000484	00000001			351                        =F' 1'
00000488	0000			352                        =H' 0'
0000048A	005F			353                        =AL2(L' MSGMSG)
				354
				355 *            some constants
				356
	00000400	00000001		357 K            EQU        1024                    One KB
	00001000	00000001		358 PAGE        EQU        (4*K)                    Size of one page
	00010000	00000001		359 K64         EQU        (64*K)                    64 KB
	00100000	00000001		360 MB          EQU        (K*K)                    1 MB
				361
	AABBCCDD	00000001		362 REG2PATT    EQU        X' AABBCCDD'            Polluted Register pattern
	000000DD	00000001		363 REG2LOW     EQU                    X' DD'            (last byte above)





LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				403	*****
				404	*            E7TEST DSECT
				405	*****
				407	E7TEST    DSECT ,
00000000	00000000			408	TSUB       DC     A(0)            pointer to test
00000004	0000			409	TNUM       DC     H' 00'           Test Number
00000006	00			410	DC     X' 00'
00000007	00			411	DC     HL1' 00'        m field - not used
				412	
00000008	40404040	40404040		413	OPNAME     DC     CL8' '           E7 name
00000010	00000000			414	V2ADDR     DC     A(0)           address of v2 source
00000014	00000000			415	V3ADDR     DC     A(0)           address of v3 source
00000018	00000000			416	RELEN       DC     A(0)           RESULT LENGTH
0000001C	00000000			417	READRR     DC     A(0)           result (expected) address
00000020	00000000	00000000		418	DS     FD               gap
00000028	00000000	00000000		419	V10OUTPUT   DS     XL16           V1 Output
00000038	00000000	00000000		420	DS     FD               gap
				421	
				422	*            test routine will be here (from VRR-c macro)
				423	*
				424	*            followed by
				425	*            EXPECTED RESULT
				427	ZVE7TST    CSECT ,
000010A8		00000000	000019E3	428	DS     0F
				430	*****
				431	*            Macros to help build test tables
				432	*****
				434	*
				435	*            macro to generate individual test
				436	*
				437	MACRO
				438	VRR_C &INST
				439	. *                                &INST    - VRR-c instruction under test
				440	. *                                no m fields
				441	
				442	GBLA   &TNUM
				443	&TNUM       SETA   &TNUM+1
				444	
				445	DS     0FD
				446	USING *, R5            base for test data and test routine
				447	
				448	T&TNUM     DC     A(X&TNUM)       address of test routine
				449	DC     H' &TNUM       test number
				450	DC     X' 00'
				451	DC     HL1' 00'        m field
				452	DC     CL8' &INST'    instruction name
				453	DC     A(RE&TNUM+16)   address of v2 source



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				502 *****	
				503 * E7 VRR-c tests	
				504 *****	
				505 PRINT DATA	
				506	
				507 * E775 VSLB - Vector Shift Left By Byte	
				508 * E77D VSRLB - Vector Shift Right Logical By Byte	
				509 * E77F VSRAB - Vector Shift Right Arithmetic By Byte	
				510	
				511 * VRR-c instruction	
				512 * followed by	
				513 * 16 byte expected result (V1)	
				514 * 16 byte V2 source	
				515 * 16 byte V3 source	
				516 * -----	
				517 * VSLB - Vector Shift Left By Byte	
				518 * -----	
				519	
000010A8				520 VRR_C VSLB	
000010A8		000010A8		521+ DS OFD	
000010A8	000010E8			522+ USING *, R5	base for test data and test routine
000010AC	0001			523+T1 DC A(X1)	address of test routine
000010AE	00			524+ DC H' 1'	test number
000010AF	00			525+ DC X' 00'	
000010B0	E5E2D3C2 40404040			526+ DC HL1' 00'	m field
000010B8	00001120			527+ DC CL8' VSLB'	instruction name
000010BC	00001130			528+ DC A(RE1+16)	address of v2 source
000010C0	00000010			529+ DC A(RE1+32)	address of v3 source
000010C4	00001110			530+ DC A(16)	result length
000010C8	00000000 00000000			531+REA1 DC A(RE1)	result address
000010D0	00000000 00000000			532+ DS FD	gap
000010D8	00000000 00000000			533+V101 DS XL16	V1 output
000010E0	00000000 00000000			534+ DS FD	gap
				535+*	
000010E8				536+X1 DS OF	
000010E8	E310 5010 0014	00000010		537+ LGF R1, V2ADDR	load v2 source
000010EE	E761 0000 0806	00000000		538+ VL v22, 0(R1)	use v22 to test decoder
000010F4	E310 5014 0014	00000014		539+ LGF R1, V3ADDR	load v3 source
000010FA	E771 0000 0806	00000000		540+ VL v23, 0(R1)	use v23 to test decoder
00001100	E766 7000 0E75			541+ VSLB V22, V22, V23	test instruction (dest is a source)
00001106	E760 5028 080E	000010D0		542+ VST V22, V101	save v1 output
0000110C	07FB			543+ BR R11	return
00001110				544+RE1 DC OF	xl16 expected result
00001110	FFFFFFFF FFFFFFFF			545+ DROP R5	
00001110	FF09FFFF FFFFFFFF			546 DC XL16' FFFFFFFFFFFFFFFFFF FF09FFFFFFFFFFFFFF'	result t
00001118	FF09FFFF FFFFFFFF				
00001120	FFFFFFFF FFFFFFFF			547 DC XL16' FFFFFFFFFFFFFFFFFF FF09FFFFFFFFFFFFFF'	v2
00001128	FF09FFFF FFFFFFFF				
00001130	00000000 00000000			548 DC XL16' 0000000000000000 0000000000000000'	v3
00001138	00000000 00000000				
				549	
00001140				550 VRR_C VSLB	
00001140		00001140		551+ DS OFD	
00001140	00001180			552+ USING *, R5	base for test data and test routine
				553+T2 DC A(X2)	address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001144	0002			554+	DC	H' 2'	test number
00001146	00			555+	DC	X' 00'	
00001147	00			556+	DC	HL1' 00'	m field
00001148	E5E2D3C2 40404040			557+	DC	CL8' VSLB'	instruction name
00001150	000011B8			558+	DC	A(RE2+16)	address of v2 source
00001154	000011C8			559+	DC	A(RE2+32)	address of v3 source
00001158	00000010			560+	DC	A(16)	result length
0000115C	000011A8			561+REA2	DC	A(RE2)	result address
00001160	00000000 00000000			562+	DS	FD	gap
00001168	00000000 00000000			563+V102	DS	XL16	V1 output
00001170	00000000 00000000						
00001178	00000000 00000000			564+	DS	FD	gap
				565+*			
00001180				566+X2	DS	0F	
00001180	E310 5010 0014		00000010	567+	LGF	R1, V2ADDR	load v2 source
00001186	E761 0000 0806		00000000	568+	VL	v22, 0(R1)	use v22 to test decoder
0000118C	E310 5014 0014		00000014	569+	LGF	R1, V3ADDR	load v3 source
00001192	E771 0000 0806		00000000	570+	VL	v23, 0(R1)	use v23 to test decoder
00001198	E766 7000 0E75			571+	VSLB	V22, V22, V23	test instruction (dest is a source)
0000119E	E760 5028 080E		00001168	572+	VST	V22, V102	save v1 output
000011A4	07FB			573+	BR	R11	return
000011A8				574+RE2	DC	0F	xl16 expected result
000011A8				575+	DROP	R5	
000011A8	FFFFFFFF FFFFFFFF			576	DC	XL16' FFFFFFFFFFFFFFFFFF 09FFFFFFFFFFFFFF00'	result
000011B0	09FFFFFF FFFFFFF00						
000011B8	FFFFFFFF FFFFFFFF			577	DC	XL16' FFFFFFFFFFFFFFFFFF FF09FFFFFFFFFFFFFF'	v2
000011C0	FF09FFFF FFFFFFFF						
000011C8	FFFFFFFF FFFFFFF08			578	DC	XL16' FFFFFFFFFFFFFFFFFF08 FFFFFFFFFFFFFFFFFF'	v3
000011D0	FFFFFFFF FFFFFFFF						
				579			
000011D8				580	VRR_C	VSLB	
000011D8		000011D8		581+	DS	0FD	
000011D8	00001218			582+	USING	*, R5	base for test data and test routine
000011DC	0003			583+T3	DC	A(X3)	address of test routine
000011DE	00			584+	DC	H' 3'	test number
000011DF	00			585+	DC	X' 00'	
000011E0	E5E2D3C2 40404040			586+	DC	HL1' 00'	m field
000011E8	00001250			587+	DC	CL8' VSLB'	instruction name
000011EC	00001260			588+	DC	A(RE3+16)	address of v2 source
000011F0	00000010			589+	DC	A(RE3+32)	address of v3 source
000011F4	00001240			590+	DC	A(16)	result length
000011F8	00000000 00000000			591+REA3	DC	A(RE3)	result address
00001200	00000000 00000000			592+	DS	FD	gap
00001208	00000000 00000000			593+V103	DS	XL16	V1 output
00001210	00000000 00000000						
				594+	DS	FD	gap
				595+*			
00001218				596+X3	DS	0F	
00001218	E310 5010 0014		00000010	597+	LGF	R1, V2ADDR	load v2 source
0000121E	E761 0000 0806		00000000	598+	VL	v22, 0(R1)	use v22 to test decoder
00001224	E310 5014 0014		00000014	599+	LGF	R1, V3ADDR	load v3 source
0000122A	E771 0000 0806		00000000	600+	VL	v23, 0(R1)	use v23 to test decoder
00001230	E766 7000 0E75			601+	VSLB	V22, V22, V23	test instruction (dest is a source)
00001236	E760 9000 080E		00001200	602+	VST	V22, V103	save v1 output
0000123C	07FB			603+	BR	R11	return
00001240				604+RE3	DC	0F	xl16 expected result



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001240				605+	DROP R5		
00001240	0F000000 00000000			606	DC XL16' 0F00000000000000 0000000000000000'	result	t
00001248	00000000 00000000						
00001250	00010203 04050607			607	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
00001258	08090A0B 0C0D0E0F						
00001260	FFFFFFFF FFFFFFFF			608	DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3	
00001268	FFFFFFFF FFFFFFFF						
				609			
00001270				610	VRR_C VSLB		
00001270		00001270		611+	DS OFD		
00001270	000012B0			612+	USING *, R5	base for test data and test routine	
00001274	0004			613+T4	DC A(X4)	address of test routine	
00001276	00			614+	DC H' 4'	test number	
00001276	00			615+	DC X' 00'		
00001277	00			616+	DC HL1' 00'	m field	
00001278	E5E2D3C2 40404040			617+	DC CL8' VSLB'	instruction name	
00001280	000012E8			618+	DC A(RE4+16)	address of v2 source	
00001284	000012F8			619+	DC A(RE4+32)	address of v3 source	
00001288	00000010			620+	DC A(16)	result length	
0000128C	000012D8			621+REA4	DC A(RE4)	result address	
00001290	00000000 00000000			622+	DS FD	gap	
00001298	00000000 00000000			623+V104	DS XL16	V1 output	
000012A0	00000000 00000000						
000012A8	00000000 00000000			624+	DS FD	gap	
				625+*			
000012B0				626+X4	DS OF		
000012B0	E310 5010 0014		00000010	627+	LGF R1, V2ADDR	load v2 source	
000012B6	E761 0000 0806		00000000	628+	VL v22, 0(R1)	use v22 to test decoder	
000012BC	E310 5014 0014		00000014	629+	LGF R1, V3ADDR	load v3 source	
000012C2	E771 0000 0806		00000000	630+	VL v23, 0(R1)	use v23 to test decoder	
000012C8	E766 7000 0E75			631+	VSLB V22, V22, V23	test instruction (dest is a source)	
000012CE	E760 5028 080E		00001298	632+	VST V22, V104	save v1 output	
000012D4	07FB			633+	BR R11	return	
000012D8				634+RE4	DC OF	xl16 expected result	
000012D8				635+	DROP R5		
000012D8	FFFFFFFF FFFFFFFF			636	DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF0000'	result	t
000012E0	FFFFFFFF FFFF0000						
000012E8	FFFFFFFF FFFFFFFF			637	DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2	
000012F0	FFFFFFFF FFFFFFFF						
000012F8	F0E0D0C0 B0A09010			638	DC XL16' F0E0D0C0B0A09010 7060504030201000'	v3	
00001300	70605040 30201000						
				639			
00001308				640	VRR_C VSLB		
00001308		00001308		641+	DS OFD		
00001308	00001348			642+	USING *, R5	base for test data and test routine	
0000130C	0005			643+T5	DC A(X5)	address of test routine	
0000130E	00			644+	DC H' 5'	test number	
0000130F	00			645+	DC X' 00'		
00001310	E5E2D3C2 40404040			646+	DC HL1' 00'	m field	
00001318	00001380			647+	DC CL8' VSLB'	instruction name	
0000131C	00001390			648+	DC A(RE5+16)	address of v2 source	
00001320	00000010			649+	DC A(RE5+32)	address of v3 source	
00001324	00001370			650+	DC A(16)	result length	
00001328	00000000 00000000			651+REA5	DC A(RE5)	result address	
00001330	00000000 00000000			652+	DS FD	gap	
				653+V105	DS XL16	V1 output	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001338	00000000 00000000							
00001340	00000000 00000000			654+	DS	FD	gap	
				655+*				
00001348				656+X5	DS	OF		
00001348	E310 5010 0014		00000010	657+	LGF	R1, V2ADDR	load v2 source	
0000134E	E761 0000 0806		00000000	658+	VL	v22, 0(R1)	use v22 to test decoder	
00001354	E310 5014 0014		00000014	659+	LGF	R1, V3ADDR	load v3 source	
0000135A	E771 0000 0806		00000000	660+	VL	v23, 0(R1)	use v23 to test decoder	
00001360	E766 7000 0E75			661+	VSLB	V22, V22, V23	test instruction (dest is a source)	
00001366	E760 5028 080E		00001330	662+	VST	V22, V105	save v1 output	
0000136C	07FB			663+	BR	R11	return	
00001370				664+RE5	DC	OF	xl16 expected result	
00001370				665+	DROP	R5		
00001370	90807060 50403020			666	DC	XL16' 9080706050403020 1000000000000000'	result t	
00001378	10000000 00000000							
00001380	F0E0D0C0 B0A09080			667	DC	XL16' F0E0D0C0B0A09080 7060504030201000'	v2	
00001388	70605040 30201000							
00001390	00000000 00000030			668	DC	XL16' 000000000000000030 0000000000000000'	v3	
00001398	00000000 00000000							
				669				
				670 *				
				671 *	VSRLB	- Vector Shift Right Logical By Byte		
				672 *				
				673				
000013A0				674	VRR_C	VSRLB		
000013A0		000013A0		675+	DS	OFD		
000013A0	000013E0			676+	USING	*, R5	base for test data and test routine	
000013A4	0006			677+T6	DC	A(X6)	address of test routine	
000013A6	00			678+	DC	H' 6'	test number	
000013A7	00			679+	DC	X' 00'		
000013A8	E5E2D9D3 C2404040			680+	DC	HL1' 00'	m field	
000013B0	00001418			681+	DC	CL8' VSRLB'	instruction name	
000013B4	00001428			682+	DC	A(RE6+16)	address of v2 source	
000013B8	00000010			683+	DC	A(RE6+32)	address of v3 source	
000013BC	00001408			684+	DC	A(16)	result length	
000013C0	00000000 00000000			685+REA6	DC	A(RE6)	result address	
000013C8	00000000 00000000			686+	DS	FD	gap	
000013D0	00000000 00000000			687+V106	DS	XL16	V1 output	
000013D8	00000000 00000000			688+	DS	FD	gap	
				689+*				
000013E0				690+X6	DS	OF		
000013E0	E310 5010 0014		00000010	691+	LGF	R1, V2ADDR	load v2 source	
000013E6	E761 0000 0806		00000000	692+	VL	v22, 0(R1)	use v22 to test decoder	
000013EC	E310 5014 0014		00000014	693+	LGF	R1, V3ADDR	load v3 source	
000013F2	E771 0000 0806		00000000	694+	VL	v23, 0(R1)	use v23 to test decoder	
000013F8	E766 7000 0E7D			695+	VSRLB	V22, V22, V23	test instruction (dest is a source)	
000013FE	E760 5028 080E		000013C8	696+	VST	V22, V106	save v1 output	
00001404	07FB			697+	BR	R11	return	
00001408				698+RE6	DC	OF	xl16 expected result	
00001408				699+	DROP	R5		
00001408	FFFFFFFF FFFFFFFF			700	DC	XL16' FFFFFFFFFFFFFFFFFF FF09FFFFFFFFFFFFFF'	result t	
00001410	FF09FFFF FFFFFFFF							
00001418	FFFFFFFF FFFFFFFF			701	DC	XL16' FFFFFFFFFFFFFFFFFF FF09FFFFFFFFFFFFFF'	v2	
00001420	FF09FFFF FFFFFFFF							
00001428	00000000 00000000			702	DC	XL16' 0000000000000000 0000000000000000'	v3	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001430	00000000 00000000			703			
				704	VRR_C	VSRLB	
00001438				705+	DS	0FD	
00001438		00001438		706+	USING	*, R5	base for test data and test routine
00001438	00001478			707+T7	DC	A(X7)	address of test routine
0000143C	0007			708+	DC	H' 7'	test number
0000143E	00			709+	DC	X' 00'	
0000143F	00			710+	DC	HL1' 00'	m field
00001440	E5E2D9D3 C2404040			711+	DC	CL8' VSRLB'	instruction name
00001448	000014B0			712+	DC	A(RE7+16)	address of v2 source
0000144C	000014C0			713+	DC	A(RE7+32)	address of v3 source
00001450	00000010			714+	DC	A(16)	result length
00001454	000014A0			715+REA7	DC	A(RE7)	result address
00001458	00000000 00000000			716+	DS	FD	gap
00001460	00000000 00000000			717+V107	DS	XL16	V1 output
00001468	00000000 00000000						
00001470	00000000 00000000			718+	DS	FD	gap
				719+*			
00001478				720+X7	DS	0F	
00001478	E310 5010 0014		00000010	721+	LGF	R1, V2ADDR	load v2 source
0000147E	E761 0000 0806		00000000	722+	VL	v22, 0(R1)	use v22 to test decoder
00001484	E310 5014 0014		00000014	723+	LGF	R1, V3ADDR	load v3 source
0000148A	E771 0000 0806		00000000	724+	VL	v23, 0(R1)	use v23 to test decoder
00001490	E766 7000 0E7D			725+	VSRLB	V22, V22, V23	test instruction (dest is a source)
00001496	E760 5028 080E		00001460	726+	VST	V22, V107	save v1 output
0000149C	07FB			727+	BR	R11	return
000014A0				728+RE7	DC	0F	xl16 expected result
000014A0				729+	DROP	R5	
000014A0	00FFFFFF FFFFFFFF			730	DC	XL16' 00FFFFFFFFFFFFFFFF FFFF09FFFFFFFFFFFF'	result
000014A8	FFFF09FF FFFFFFFF						
000014B0	FFFFFFFF FFFFFFFF			731	DC	XL16' FFFFFFFFFFFFFFFFFF FF09FFFFFFFFFFFF'	v2
000014B8	FF09FFFF FFFFFFFF						
000014C0	FFFFFFFF FFFFFF08			732	DC	XL16' FFFFFFFFFFFFFFFFFF08 FFFFFFFFFFFFFFFFFF'	v3
000014C8	FFFFFFFF FFFFFFFF						
				733			
000014D0				734	VRR_C	VSRLB	
000014D0		000014D0		735+	DS	0FD	
000014D0	00001510			736+	USING	*, R5	base for test data and test routine
000014D4	0008			737+T8	DC	A(X8)	address of test routine
000014D6	00			738+	DC	H' 8'	test number
000014D7	00			739+	DC	X' 00'	
000014D8	E5E2D9D3 C2404040			740+	DC	HL1' 00'	m field
000014E0	00001548			741+	DC	CL8' VSRLB'	instruction name
000014E4	00001558			742+	DC	A(RE8+16)	address of v2 source
000014E8	00000010			743+	DC	A(RE8+32)	address of v3 source
000014EC	00001538			744+	DC	A(16)	result length
000014F0	00000000 00000000			745+REA8	DC	A(RE8)	result address
000014F8	00000000 00000000			746+	DS	FD	gap
00001500	00000000 00000000			747+V108	DS	XL16	V1 output
00001508	00000000 00000000						
				748+	DS	FD	gap
				749+*			
00001510				750+X8	DS	0F	
00001510	E310 5010 0014		00000010	751+	LGF	R1, V2ADDR	load v2 source
00001516	E761 0000 0806		00000000	752+	VL	v22, 0(R1)	use v22 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000151C	E310 5014 0014		00000014	753+	LGF	R1, V3ADDR	load v3 source
00001522	E771 0000 0806		00000000	754+	VL	v23, 0(R1)	use v23 to test decoder
00001528	E766 7000 0E7D			755+	VSRLB	V22, V22, V23	test instruction (dest is a source)
0000152E	E760 5028 080E		000014F8	756+	VST	V22, V108	save v1 output
00001534	07FB			757+	BR	R11	return
00001538				758+RE8	DC	0F	xl16 expected result
00001538				759+	DROP	R5	
00001538	00000000 00000000			760	DC	XL16' 0000000000000000 0000000000000080'	result t
00001540	00000000 00000080						
00001548	80010203 04050607			761	DC	XL16' 8001020304050607 08090A0B0C0D0E0F'	v2
00001550	08090A0B 0C0D0E0F						
00001558	FFFFFFFF FFFFFFFF			762	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
00001560	FFFFFFFF FFFFFFFF						
				763			
				764	VRR_C	VSRLB	
00001568				765+	DS	0FD	
00001568		00001568		766+	USING	*, R5	base for test data and test routine
00001568	000015A8			767+T9	DC	A(X9)	address of test routine
0000156C	0009			768+	DC	H' 9'	test number
0000156E	00			769+	DC	X' 00'	
0000156F	00			770+	DC	HL1' 00'	m field
00001570	E5E2D9D3 C2404040			771+	DC	CL8' VSRLB'	instruction name
00001578	000015E0			772+	DC	A(RE9+16)	address of v2 source
0000157C	000015F0			773+	DC	A(RE9+32)	address of v3 source
00001580	00000010			774+	DC	A(16)	result length
00001584	000015D0			775+REA9	DC	A(RE9)	result address
00001588	00000000 00000000			776+	DS	FD	gap
00001590	00000000 00000000			777+V109	DS	XL16	V1 output
00001598	00000000 00000000						
000015A0	00000000 00000000			778+	DS	FD	gap
				779+*			
000015A8				780+X9	DS	0F	
000015A8	E310 5010 0014		00000010	781+	LGF	R1, V2ADDR	load v2 source
000015AE	E761 0000 0806		00000000	782+	VL	v22, 0(R1)	use v22 to test decoder
000015B4	E310 5014 0014		00000014	783+	LGF	R1, V3ADDR	load v3 source
000015BA	E771 0000 0806		00000000	784+	VL	v23, 0(R1)	use v23 to test decoder
000015C0	E766 7000 0E7D			785+	VSRLB	V22, V22, V23	test instruction (dest is a source)
000015C6	E760 5028 080E		00001590	786+	VST	V22, V109	save v1 output
000015CC	07FB			787+	BR	R11	return
000015D0				788+RE9	DC	0F	xl16 expected result
000015D0				789+	DROP	R5	
000015D0	0000FFFF FFFFFFFF			790	DC	XL16' 0000FFFFFFFFFFFFFFFF FF09FFFFFFFFFFFFFF'	result t
000015D8	FFFFFFFF09 FFFFFFFF						
000015E0	FFFFFFFF FFFFFFFF			791	DC	XL16' FFFFFFFFFFFFFFFFFF FF09FFFFFFFFFFFFFF'	v2
000015E8	FF09FFFF FFFFFFFF						
000015F0	F0E0D0C0 B0A09010			792	DC	XL16' F0E0D0C0B0A09010 7060504030201000'	v3
000015F8	70605040 30201000						
				793			
				794	VRR_C	VSRLB	
00001600				795+	DS	0FD	
00001600		00001600		796+	USING	*, R5	base for test data and test routine
00001600	00001640			797+T10	DC	A(X10)	address of test routine
00001604	000A			798+	DC	H' 10'	test number
00001606	00			799+	DC	X' 00'	
00001607	00			800+	DC	HL1' 00'	m field
00001608	E5E2D9D3 C2404040			801+	DC	CL8' VSRLB'	instruction name



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001610	00001678			802+	DC	A(RE10+16)	address of v2 source
00001614	00001688			803+	DC	A(RE10+32)	address of v3 source
00001618	00000010			804+	DC	A(16)	result length
0000161C	00001668			805+REA10	DC	A(RE10)	result address
00001620	00000000 00000000			806+	DS	FD	gap
00001628	00000000 00000000			807+V1010	DS	XL16	V1 output
00001630	00000000 00000000						
00001638	00000000 00000000			808+	DS	FD	gap
				809+*			
00001640				810+X10	DS	0F	
00001640	E310 5010 0014		00000010	811+	LGF	R1, V2ADDR	load v2 source
00001646	E761 0000 0806		00000000	812+	VL	v22, 0(R1)	use v22 to test decoder
0000164C	E310 5014 0014		00000014	813+	LGF	R1, V3ADDR	load v3 source
00001652	E771 0000 0806		00000000	814+	VL	v23, 0(R1)	use v23 to test decoder
00001658	E766 7000 0E7D			815+	VSRLB	V22, V22, V23	test instruction (dest is a source)
0000165E	E760 5028 080E		00001628	816+	VST	V22, V1010	save v1 output
00001664	07FB			817+	BR	R11	return
00001668				818+RE10	DC	0F	xl16 expected result
00001668				819+	DROP	R5	
00001668	00000000 0000F0E0			820	DC	XL16' 000000000000F0E0 D0C0B0A090807060'	result t
00001670	D0C0B0A0 90807060						
00001678	F0E0D0C0 B0A09080			821	DC	XL16' F0E0D0C0B0A09080 7060504030201000'	v2
00001680	70605040 30201000						
00001688	00000000 00000030			822	DC	XL16' 0000000000000030 0000000000000000'	v3
00001690	00000000 00000000						
				823			
				824 *			
				825 *	VSRAB	- Vector Shift Right Arithmetic By Byte	
				826 *			
				827			
00001698				828	VRR_C	VSRAB	
00001698		00001698		829+	DS	0FD	
00001698	000016D8			830+	USING	*, R5	base for test data and test routine
0000169C	000B			831+T11	DC	A(X11)	address of test routine
0000169E	00			832+	DC	H' 11'	test number
0000169F	00			833+	DC	X' 00'	
000016A0	E5E2D9C1 C2404040			834+	DC	HL1' 00'	m field
000016A8	00001710			835+	DC	CL8' VSRAB'	instruction name
000016AC	00001720			836+	DC	A(RE11+16)	address of v2 source
000016B0	00000010			837+	DC	A(RE11+32)	address of v3 source
000016B4	00001700			838+	DC	A(16)	result length
000016B8	00000000 00000000			839+REA11	DC	A(RE11)	result address
000016C0	00000000 00000000			840+	DS	FD	gap
000016C8	00000000 00000000			841+V1011	DS	XL16	V1 output
000016D0	00000000 00000000						
				842+	DS	FD	gap
				843+*			
000016D8				844+X11	DS	0F	
000016D8	E310 5010 0014		00000010	845+	LGF	R1, V2ADDR	load v2 source
000016DE	E761 0000 0806		00000000	846+	VL	v22, 0(R1)	use v22 to test decoder
000016E4	E310 5014 0014		00000014	847+	LGF	R1, V3ADDR	load v3 source
000016EA	E771 0000 0806		00000000	848+	VL	v23, 0(R1)	use v23 to test decoder
000016F0	E766 7000 0E7F			849+	VSRAB	V22, V22, V23	test instruction (dest is a source)
000016F6	E760 5028 080E		000016C0	850+	VST	V22, V1011	save v1 output
000016FC	07FB			851+	BR	R11	return
00001700				852+RE11	DC	0F	xl16 expected result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001700				853+	DROP R5		
00001700	FFFFFFFF FFFFFFFF			854	DC	XL16' FFFFFFFFFFFFFFFFFF FF09FFFFFFFFFFFF'	result
00001708	FF09FFFF FFFFFFFF						
00001710	FFFFFFFF FFFFFFFF			855	DC	XL16' FFFFFFFFFFFFFFFFFF FF09FFFFFFFFFFFF'	v2
00001718	FF09FFFF FFFFFFFF						
00001720	00000000 00000000			856	DC	XL16' 0000000000000000 0000000000000000'	v3
00001728	00000000 00000000						
				857			
				858	VRR_C VSRAB		
00001730				859+	DS OFD		
00001730		00001730		860+	USING *, R5	base for test data and test routine	
00001730	00001770			861+T12	DC A(X12)	address of test routine	
00001734	000C			862+	DC H' 12'	test number	
00001736	00			863+	DC X' 00'		
00001737	00			864+	DC HL1' 00'	m field	
00001738	E5E2D9C1 C2404040			865+	DC CL8' VSRAB'	instruction name	
00001740	000017A8			866+	DC A(RE12+16)	address of v2 source	
00001744	000017B8			867+	DC A(RE12+32)	address of v3 source	
00001748	00000010			868+	DC A(16)	result length	
0000174C	00001798			869+REA12	DC A(RE12)	result address	
00001750	00000000 00000000			870+	DS FD	gap	
00001758	00000000 00000000			871+V1012	DS XL16	V1 output	
00001760	00000000 00000000						
00001768	00000000 00000000			872+	DS FD	gap	
				873+*			
00001770				874+X12	DS OF		
00001770	E310 5010 0014		00000010	875+	LGF R1, V2ADDR	load v2 source	
00001776	E761 0000 0806		00000000	876+	VL v22, 0(R1)	use v22 to test decoder	
0000177C	E310 5014 0014		00000014	877+	LGF R1, V3ADDR	load v3 source	
00001782	E771 0000 0806		00000000	878+	VL v23, 0(R1)	use v23 to test decoder	
00001788	E766 7000 0E7F			879+	VSRAB V22, V22, V23	test instruction (dest is a source)	
0000178E	E760 5028 080E		00001758	880+	VST V22, V1012	save v1 output	
00001794	07FB			881+	BR R11	return	
00001798				882+RE12	DC OF	xl16 expected result	
00001798				883+	DROP R5		
00001798	FFFFFFFF FFFFFFFF			884	DC	XL16' FFFFFFFFFFFFFFFFFF FFFF09FFFFFFFFFFFF'	result
000017A0	FFFF09FF FFFFFFFF						
000017A8	FFFFFFFF FFFFFFFF			885	DC	XL16' FFFFFFFFFFFFFFFFFF FF09FFFFFFFFFFFF'	v2
000017B0	FF09FFFF FFFFFFFF						
000017B8	FFFFFFFF FFFFFFFF08			886	DC	XL16' FFFFFFFFFFFFFFFFFF08 FFFFFFFFFFFFFFFFFF'	v3
000017C0	FFFFFFFF FFFFFFFF						
				887			
				888	VRR_C VSRAB		
000017C8				889+	DS OFD		
000017C8		000017C8		890+	USING *, R5	base for test data and test routine	
000017C8	00001808			891+T13	DC A(X13)	address of test routine	
000017CC	000D			892+	DC H' 13'	test number	
000017CE	00			893+	DC X' 00'		
000017CF	00			894+	DC HL1' 00'	m field	
000017D0	E5E2D9C1 C2404040			895+	DC CL8' VSRAB'	instruction name	
000017D8	00001840			896+	DC A(RE13+16)	address of v2 source	
000017DC	00001850			897+	DC A(RE13+32)	address of v3 source	
000017E0	00000010			898+	DC A(16)	result length	
000017E4	00001830			899+REA13	DC A(RE13)	result address	
000017E8	00000000 00000000			900+	DS FD	gap	
000017F0	00000000 00000000			901+V1013	DS XL16	V1 output	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000017F8	00000000 00000000						
00001800	00000000 00000000			902+	DS	FD	gap
				903+*			
00001808				904+X13	DS	0F	
00001808	E310 5010 0014		00000010	905+	LGF	R1, V2ADDR	load v2 source
0000180E	E761 0000 0806		00000000	906+	VL	v22, 0(R1)	use v22 to test decoder
00001814	E310 5014 0014		00000014	907+	LGF	R1, V3ADDR	load v3 source
0000181A	E771 0000 0806		00000000	908+	VL	v23, 0(R1)	use v23 to test decoder
00001820	E766 7000 0E7F			909+	VSRAB	V22, V22, V23	test instruction (dest is a source)
00001826	E760 5028 080E		000017F0	910+	VST	V22, V1013	save v1 output
0000182C	07FB			911+	BR	R11	return
00001830				912+RE13	DC	0F	xl16 expected result
00001830				913+	DROP	R5	
00001830	FFFFFFFF FFFFFFFF			914	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF80'	result t
00001838	FFFFFFFF FFFFFFFF80						
00001840	80010203 04050607			915	DC	XL16' 8001020304050607 08090A0B0C0D0E0F'	v2
00001848	08090A0B 0C0D0E0F						
00001850	FFFFFFFF FFFFFFFF			916	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
00001858	FFFFFFFF FFFFFFFF						
				917			
00001860				918	VRR_C	VSRAB	
00001860		00001860		919+	DS	0FD	
00001860	000018A0			920+	USING	*, R5	base for test data and test routine
00001864	000E			921+T14	DC	A(X14)	address of test routine
00001866	00			922+	DC	H' 14'	test number
00001867	00			923+	DC	X' 00'	
00001868	E5E2D9C1 C2404040			924+	DC	HL1' 00'	m field
00001870	000018D8			925+	DC	CL8' VSRAB'	instruction name
00001874	000018E8			926+	DC	A(RE14+16)	address of v2 source
00001878	00000010			927+	DC	A(RE14+32)	address of v3 source
0000187C	000018C8			928+	DC	A(16)	result length
00001880	00000000 00000000			929+REA14	DC	A(RE14)	result address
00001888	00000000 00000000			930+	DS	FD	gap
00001890	00000000 00000000			931+V1014	DS	XL16	V1 output
00001898	00000000 00000000			932+	DS	FD	gap
				933+*			
000018A0				934+X14	DS	0F	
000018A0	E310 5010 0014		00000010	935+	LGF	R1, V2ADDR	load v2 source
000018A6	E761 0000 0806		00000000	936+	VL	v22, 0(R1)	use v22 to test decoder
000018AC	E310 5014 0014		00000014	937+	LGF	R1, V3ADDR	load v3 source
000018B2	E771 0000 0806		00000000	938+	VL	v23, 0(R1)	use v23 to test decoder
000018B8	E766 7000 0E7F			939+	VSRAB	V22, V22, V23	test instruction (dest is a source)
000018BE	E760 5028 080E		00001888	940+	VST	V22, V1014	save v1 output
000018C4	07FB			941+	BR	R11	return
000018C8				942+RE14	DC	0F	xl16 expected result
000018C8				943+	DROP	R5	
000018C8	000040FF FFFFFFFF			944	DC	XL16' 000040FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
000018D0	FFFFFFFF FFFFFFFF						
000018D8	40FFFFFFFF FFFFFFFF			945	DC	XL16' 40FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
000018E0	FFFFFFFF FFFFFFFF						
000018E8	F0E0D0C0 B0A09010			946	DC	XL16' F0E0D0C0B0A09010 7060504030201000'	v3
000018F0	70605040 30201000						
				947			
				948	VRR_C	VSRAB	
000018F8				949+	DS	0FD	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000018F8		000018F8		950+	USING *,R5	base for test data and test routine
000018F8	00001938			951+T15	DC A(X15)	address of test routine
000018FC	000F			952+	DC H' 15'	test number
000018FE	00			953+	DC X' 00'	
000018FF	00			954+	DC HL1' 00'	m field
00001900	E5E2D9C1 C2404040			955+	DC CL8' VSRAB'	instruction name
00001908	00001970			956+	DC A(RE15+16)	address of v2 source
0000190C	00001980			957+	DC A(RE15+32)	address of v3 source
00001910	00000010			958+	DC A(16)	result length
00001914	00001960			959+REA15	DC A(RE15)	result address
00001918	00000000 00000000			960+	DS FD	gap
00001920	00000000 00000000			961+V1015	DS XL16	V1 output
00001928	00000000 00000000					
00001930	00000000 00000000			962+	DS FD	gap
				963+*		
00001938				964+X15	DS 0F	
00001938	E310 5010 0014	00000010		965+	LGF R1, V2ADDR	load v2 source
0000193E	E761 0000 0806	00000000		966+	VL v22, 0(R1)	use v22 to test decoder
00001944	E310 5014 0014	00000014		967+	LGF R1, V3ADDR	load v3 source
0000194A	E771 0000 0806	00000000		968+	VL v23, 0(R1)	use v23 to test decoder
00001950	E766 7000 0E7F			969+	VSRAB V22, V22, V23	test instruction (dest is a source)
00001956	E760 5028 080E	00001920		970+	VST V22, V1015	save v1 output
0000195C	07FB			971+	BR R11	return
00001960				972+RE15	DC 0F	xl16 expected result
00001960				973+	DROP R5	
00001960	00000000 000070E0			974	DC XL16' 0000000000000070E0 D0C0B0A090807060'	result t
00001968	D0C0B0A0 90807060					
00001970	70E0D0C0 B0A09080			975	DC XL16' 70E0D0C0B0A09080 7060504030201000'	v2
00001978	70605040 30201000					
00001980	00000000 00000030			976	DC XL16' 00000000000000030 0000000000000000'	v3
00001988	00000000 00000000					
				977		
00001990	00000000			978	DC F' 0'	END OF TABLE
00001994	00000000			979	DC F' 0'	
				980 *		
				981 *	table of pointers to individual load test	
				982 *		
00001998				983 E7TESTS	DS 0F	
				984	PTTABLE	
00001998				985+TTABLE	DS 0F	
00001998	000010A8			986+	DC A(T1)	
0000199C	00001140			987+	DC A(T2)	
000019A0	000011D8			988+	DC A(T3)	
000019A4	00001270			989+	DC A(T4)	
000019A8	00001308			990+	DC A(T5)	
000019AC	000013A0			991+	DC A(T6)	
000019B0	00001438			992+	DC A(T7)	
000019B4	000014D0			993+	DC A(T8)	
000019B8	00001568			994+	DC A(T9)	
000019BC	00001600			995+	DC A(T10)	
000019C0	00001698			996+	DC A(T11)	
000019C4	00001730			997+	DC A(T12)	
000019C8	000017C8			998+	DC A(T13)	
000019CC	00001860			999+	DC A(T14)	
000019D0	000018F8			1000+	DC A(T15)	
				1001+*		



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				1008	*****
				1009	*            Register equates
				1010	*****
		00000000	00000001	1012 R0	EQU 0
		00000001	00000001	1013 R1	EQU 1
		00000002	00000001	1014 R2	EQU 2
		00000003	00000001	1015 R3	EQU 3
		00000004	00000001	1016 R4	EQU 4
		00000005	00000001	1017 R5	EQU 5
		00000006	00000001	1018 R6	EQU 6
		00000007	00000001	1019 R7	EQU 7
		00000008	00000001	1020 R8	EQU 8
		00000009	00000001	1021 R9	EQU 9
		0000000A	00000001	1022 R10	EQU 10
		0000000B	00000001	1023 R11	EQU 11
		0000000C	00000001	1024 R12	EQU 12
		0000000D	00000001	1025 R13	EQU 13
		0000000E	00000001	1026 R14	EQU 14
		0000000F	00000001	1027 R15	EQU 15
				1029	*****
				1030	*            Register equates
				1031	*****
		00000000	00000001	1033 V0	EQU 0
		00000001	00000001	1034 V1	EQU 1
		00000002	00000001	1035 V2	EQU 2
		00000003	00000001	1036 V3	EQU 3
		00000004	00000001	1037 V4	EQU 4
		00000005	00000001	1038 V5	EQU 5
		00000006	00000001	1039 V6	EQU 6
		00000007	00000001	1040 V7	EQU 7
		00000008	00000001	1041 V8	EQU 8
		00000009	00000001	1042 V9	EQU 9
		0000000A	00000001	1043 V10	EQU 10
		0000000B	00000001	1044 V11	EQU 11
		0000000C	00000001	1045 V12	EQU 12
		0000000D	00000001	1046 V13	EQU 13
		0000000E	00000001	1047 V14	EQU 14
		0000000F	00000001	1048 V15	EQU 15
		00000010	00000001	1049 V16	EQU 16
		00000011	00000001	1050 V17	EQU 17
		00000012	00000001	1051 V18	EQU 18
		00000013	00000001	1052 V19	EQU 19
		00000014	00000001	1053 V20	EQU 20
		00000015	00000001	1054 V21	EQU 21





SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES				
R6	U	00000006	1	1018					
R7	U	00000007	1	1019					
R8	U	00000008	1	1020	152	156	157	158	160
R9	U	00000009	1	1021	153	160	161	163	
RE1	F	00001110	4	544	528	529	531		
RE10	F	00001668	4	818	802	803	805		
RE11	F	00001700	4	852	836	837	839		
RE12	F	00001798	4	882	866	867	869		
RE13	F	00001830	4	912	896	897	899		
RE14	F	000018C8	4	942	926	927	929		
RE15	F	00001960	4	972	956	957	959		
RE2	F	000011A8	4	574	558	559	561		
RE3	F	00001240	4	604	588	589	591		
RE4	F	000012D8	4	634	618	619	621		
RE5	F	00001370	4	664	648	649	651		
RE6	F	00001408	4	698	682	683	685		
RE7	F	000014A0	4	728	712	713	715		
RE8	F	00001538	4	758	742	743	745		
RE9	F	000015D0	4	788	772	773	775		
REA1	A	000010C4	4	531					
REA10	A	0000161C	4	805					
REA11	A	000016B4	4	839					
REA12	A	0000174C	4	869					
REA13	A	000017E4	4	899					
REA14	A	0000187C	4	929					
REA15	A	00001914	4	959					
REA2	A	0000115C	4	561					
REA3	A	000011F4	4	591					
REA4	A	0000128C	4	621					
REA5	A	00001324	4	651					
REA6	A	000013BC	4	685					
REA7	A	00001454	4	715					
REA8	A	000014EC	4	745					
REA9	A	00001584	4	775					
READDR	A	0000001C	4	417	224				
REG2LOW	U	000000DD	1	363					
REG2PATT	U	AABBCCDD	1	362					
RELEN	A	00000018	4	416					
RPTDWSAV	D	00000380	8	288	275	279			
RPTERROR	I	0000032C	4	262	237				
RPTSAVE	F	00000374	4	285	262	282			
RPTSVR5	F	00000378	4	286	263	281			
SKL0001	U	0000004E	1	182	198				
SKT0001	C	0000022A	20	179	182	199			
SVOLDPSW	U	00000140	0	118					
T1	A	000010A8	4	523	986				
T10	A	00001600	4	797	995				
T11	A	00001698	4	831	996				
T12	A	00001730	4	861	997				
T13	A	000017C8	4	891	998				
T14	A	00001860	4	921	999				
T15	A	000018F8	4	951	1000				
T2	A	00001140	4	553	987				
T3	A	000011D8	4	583	988				
T4	A	00001270	4	613	989				
T5	A	00001308	4	643	990				









DESC	SYMBOL	SIZE	POS	ADDR
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Entry: 0

Image Region CSECT	IMAGE	6628	0000-19E3	0000-19E3
		6628	0000-19E3	0000-19E3
	ZVE7TST	6628	0000-19E3	0000-19E3

STM	FILE NAME
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1	/home/tn529/sharedvfp/tests/zvector-e7-15-ShiftByByte.asm
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**\*\* NO ERRORS FOUND \*\***